Advanced Channel Engineering Achieving Aggressive Reduction of V_T Variation for Ultra-Low-Power Applications

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Abstract

We have achieved aggressive reduction of V_T variation and $V_{DD\text{-}min}$ by a sophisticated planar bulk MOSFET named 'Deeply Depleted Channel™ (DDC)'. The DDC transistor has been successfully integrated into an existing 65nm CMOS platform by combining layered channel formation and low temperature processing. The 2x reduction of V_T variation in 65nm-node has been demonstrated by matching SRAM pair transistors, 2x improvement in SRAM static noise margin (SNM) and 300 mV $V_{DD\text{-}min}$ reduction of 576Kb SRAM macros to 0.425 V using conventional 6T cell layout.

Introduction

Power consumption of scaled CMOS is a big issue. Ultra-low-voltage operation is very effective to reduce both static and dynamic power. However, ultra-low-voltage operation is limited by V_T variation as widely discussed for SRAM [1].

V_T variation has two components, inter-die and intra-die variation. The former is caused by manufacturing fluctuation such as CD variation and can be compensated by design techniques such as adaptive Vbb control. On the other hand, the latter is caused by physical mechanisms such as random dopant fluctuation (RDF) [2], line edge roughness (LER) [3] and poly grain granularity (PGG) [4].

RDF is the dominant mechanism of intra die V_T variation. New structures such as ETSOI [5], Tri-gate FET [6] and delta-doped channel bulk MOSFET [7] were proposed to solve RDF. Among the structures, delta-doped channel bulk MOSFET is the most desirable solution because it very easily matches with adaptive Vbb control independently applicable to both NMOS and PMOS, simple planar manufacturing infrastructure and existing IP design layouts including multiple V_T and legacy transistors.

Epitaxial channel selectively grown after STI was proposed to realize the delta-doped channel bulk MOSFET [8, 9]. However the prior articles focused on capability to achieve higher performance and shorter channel rather than reduction of V_T variation. Moreover, selectively grown epitaxial Si has facet at the edge of active area which may generate parasitic leakage.

In this paper, we report 1) DDC structure achieving 2x reduction of V_T variation, 2) combination of layered channel formation and low temperature process flow realizing DDC transistor, 3) 65nm SRAM results demonstrating the aggressive reduction of V_T variation by DDC and its capability of ultra-low-voltage operation.

DDC Transistor Structure

Cross sectional TEM of fabricated DDC transistor is shown in Fig. 1(a) and sketch of it is shown in Fig. 1(b). Several layers are stacked in usual P or Nwell formed in bulk silicon substrate. Layer 4 serves to prevent sub-channel punch-through. Layer 3 is the screening layer, which terminates the depletion layer in the channel and also serves to smooth the depletion layer across the device, affording excellent σV_T and short channel effects. Layer 2 is V_T setting layer that allows multiple threshold voltage devices, which are highly desired for many SoC applications. Together, these three deep layers also produce a strong body coefficient that matches adaptive Vbb control and enables many circuit level power reduction techniques. Layer 1 is a very low doped channel that reduces RDF. A key benefit of the DDC architecture is that it is fully compatible with all known transistor performance enablers including PMOS embedded SiGe S/D. The devices reported here also utilized a tensile capping layer to enhance NMOS performance as seen in Fig. 1(a).

Features of Process Flow and Verification of Them

Process flow to fabricate DDC transistor is shown in Fig. 2. The process flow serves not only low voltage (LV) operating DDC transistors but also high voltage (HV) operating legacy transistors such as 3.3V I/O transistors. Layer 1 is formed by state of the art blanket undoped epitaxial deposition, giving excellent uniformity and allowing for near perfect thickness control across a wafer. This layer is grown after forming the layered channel stack by implantation and before STI. STI and gate oxidation (GOX) for both HV and LV transistors are done at very low temperature to prevent the impurity profiles in the channel stack from diffusing. No halo implant is done for DDC transistors. Steps for doping and activating gate, source/drain are set as same as baseline 65nm process not to cause gate depletion nor increased parasitic source drain resistance.

Since all process conditions except reduced thermal budget for STI & GOX were set as same as baseline 65nm technology, concerns of the process flow are focused on items related to low temperature STI & GOX.

Cross-sectional TEM picture of STI is shown in Fig. 3. Though increased STI recess and/or divot due to low temperature process were concerned, excellent STI shape has been achieved by optimizing other parameters for the STI process.

W dependence of V_T is shown in Fig. 4. No abnormality is seen. Sub-threshold characteristics of both NMOS and PMOS

DDC are shown in Fig. 5. No kink of sub-threshold characteristics is seen. These results demonstrate no parasitic leakage path along STI edge because of blanket epitaxial layer and optimized low temperature STI process.

Distribution of breakdown voltage for low temperature gate dielectric on DDC transistor is shown in Fig. 6. No concern is seen. HCI of NMOS and PMOS DDC results are shown in Fig. 7. Estimated lifetimes are long enough even for 1.2V applications. NBTI of PMOS DDC is shown in Fig. 8. Estimated lifetime is long enough even for 1.2V applications. These results demonstrate no concern about reliability due to the low temperature GOX process.

65nm SRAM Evaluation Results

Because SRAM is the severest circuit for ultra-low voltage operation, it is the best to demonstrate capability of DDC transistors to achieve aggressive reduction of V_T variation and ultra-low voltage operation. Data on DDC transistors are compared with the ones on existing baseline 65nm control wafer using a same SRAM macro. The SRAM macro, which is in production for our 65nm ASIC offering, was used for the control and DDC wafers with no layout or design changes.

Fig. 9(a-c) shows across-wafer V_T distributions of 3 types of 6T SRAM cell transistors. These data represents inter-die V_T variation. Much tighter V_T distribution of DDC than control has been demonstrated although NMOS V_T of DDC wafer in this experiment was deviated from control. Fig. 9(d) illustrates that inter-die V_T variation is reduced to half by DDC transistor. The result demonstrates not only excellent capability of DDC transistor itself but also excellent uniformity of process parameters across a wafer such as epitaxial layer and low temperature GOX thickness.

Fig. 10(a-c) shows distributions of V_T matching for 3 types of pair transistors forming 6T SRAM cell. These data represents intra-die V_T variation. Fig. 10(d) illustrates that intra-die V_T variation is reduced to half by DDC transistor. The result demonstrates not only excellent capability of DDC transistor itself but also the low temperature process flow successfully achieving ideal DDC channel profiles reducing RDF.

Fig. 11(a-b) shows superposition of 6T SRAM butterfly curves on DDC and control wafers. Much clearer butterfly curve of DDC than control at low V_{dd} region is seen. Smaller SNM of DDC than control at high V_{dd} region is caused by lower NMOS V_T of DDC in this experiment than control and is improved by adjusting NMOS V_T.

Fig. 12(a-b) shows distribution of SNM within each of DDC and control wafers. Both distributions are nice normal distributions and it is clear that the distribution of DDC is much tighter than control.

Fig. 13(a-b) shows the measured mean & sigma SNM as a function of V_{dd}, and demonstrates that SNM variation is aggressively reduced to half by DDC transistor. Fig. 13(c) shows mean/1σ of SNM as a function of V_{dd}. It is required to keep >5σ margin for 1Mb SRAM function. DDC transistor has sufficient margin even if V_{dd}=0.4 V.

Fig. 14 shows functional yield of 576Kb SRAM macros as a function of V_{dd}. The yield means no fail bit in 576Kb SRAM array. The DDC showed good yield down to V_{dd}=0.425 V, 300 mV lower than the control, as predicted by the measured SNM results shown in Fig. 13(c).

All these results consistently demonstrate both outstanding capability of DDC transistor for ultra-low-voltage applications and manufacturability of it.

Conclusions

A new planar transistor architecture (DDC) has been successfully fabricated for the first time by combination of layered channel formation and low temperature processing. The new process was shown to not affect critical performance parameters such as parasitic leakage along STI edge and gate insulator related reliability. The DDC transistor is promising for ultra-low power applications as shown by 2x improvement in inter-die and intra-die V_T variation and 2x improvement in 6T SRAM SNM. We have demonstrated 300mV $V_{DD\text{-}min}$ reduction and fully functional 576Kb SRAM down to 0.425V.

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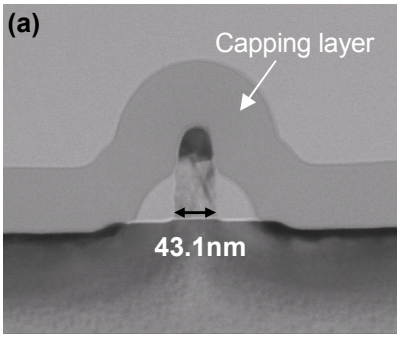

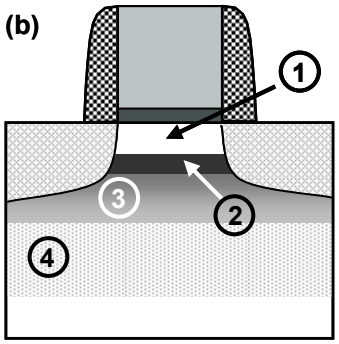

Fig.1 (a) Cross-sectional TEM picture of DDC transistor, (b) Cross sectional sketch of DDC transistor.

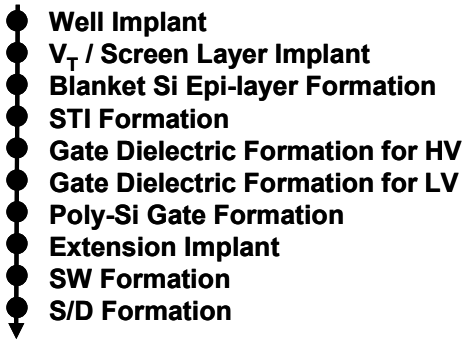

Fig.2 DDC process flow with low-temperature STI & GOX

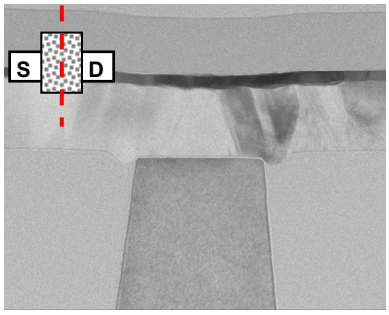

Fig.3 Cross-sectional TEM picture of STI formed by low-temperature process.

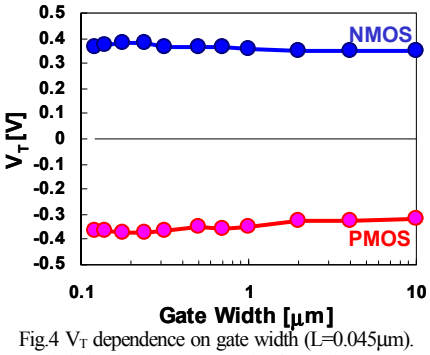

Fig.4 V_T dependence on gate width (L=0.045μm). V_T is defined as V_g at I_d=3E-6*W/L [A] for NMOS and -1E-6 for PMOS.

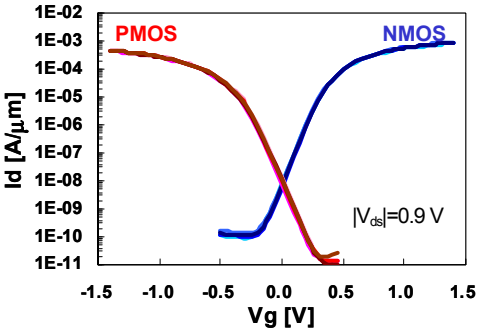

Fig.5 V_g-I_d curves of DDC (W/L=1/0.045 μm).

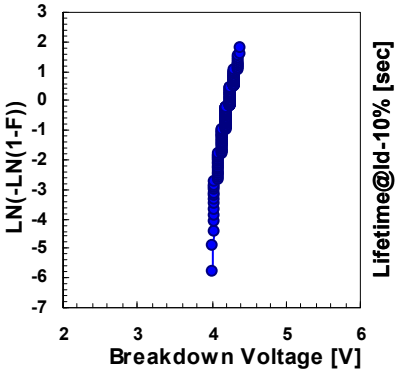

Fig.6 VRDB results of LV gate dielectric. W/L=5/0.045 μm. S_g=1E-7 cm^2.

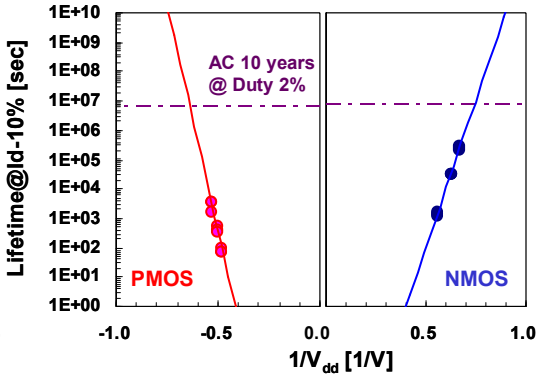

Fig.7 HCI results of NMOS and PMOS DDC at T=25C. W/L=10/0.045μm.

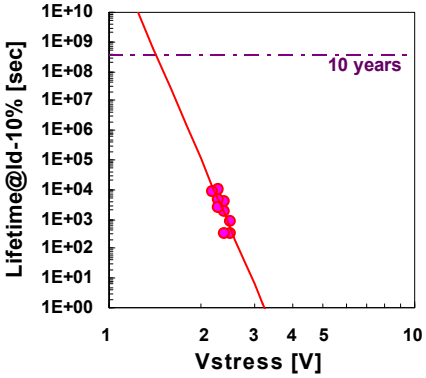

Fig.8 NBTI result of PMOS DDC at T=125C. W/L=10/0.045μm.

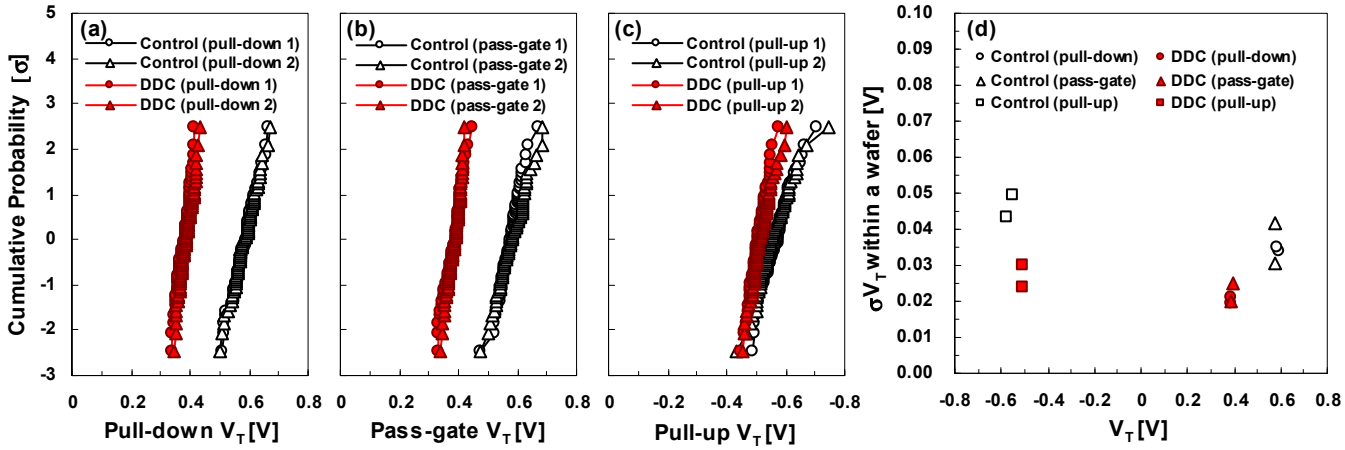

Fig.9 Across-wafer V_T distributions of (a) pull-down, (b) pass-gate and (c) pull-up. (d) Inter-die V_T variation as a function of V_T at V_{dd}=1.2V. V_T is defined as V_g at Ids=3E-6*W/L[A] for NMOS and 1E-6 for PMOS.

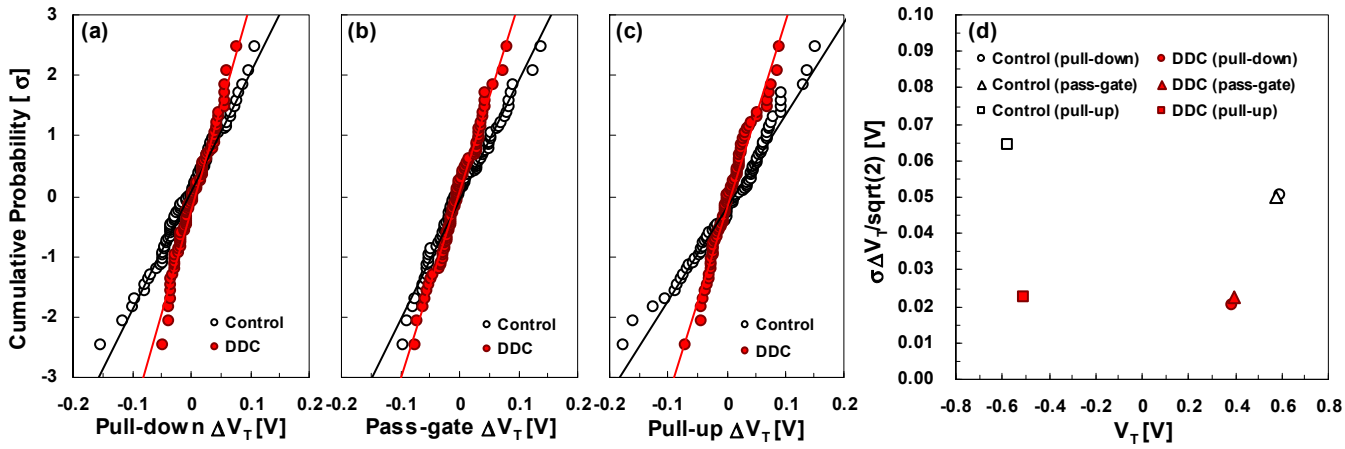

Fig.10 Distribution of V_T matching for (a) pull-down pairs, (b) pass-gate pairs and (c) pull-up pairs within a wafer. (d) Intra die V_T variation as a function of V_T at V_{dd}=1.2V. V_T is defined as V_g at Ids=3E-6*W/L [A] for NMOS and 1E-6 for PMOS.

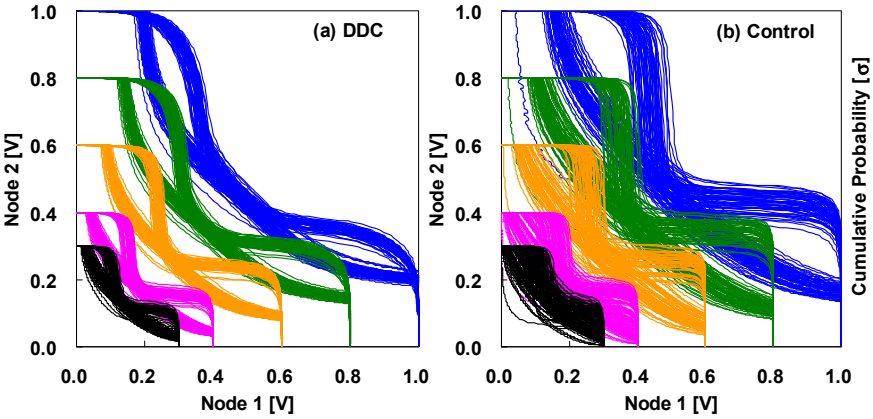

Fig.11 Superposed butterfly curves of 65nm-node SRAM cell (0.54 μm^2) on (a) DDC and (b) control.

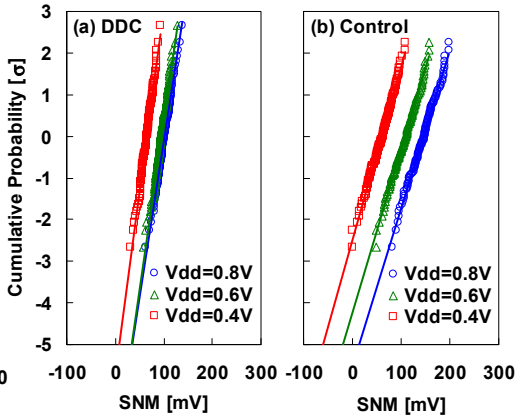

Fig.12 Distribution of SNM for (a) DDC and (b) control.

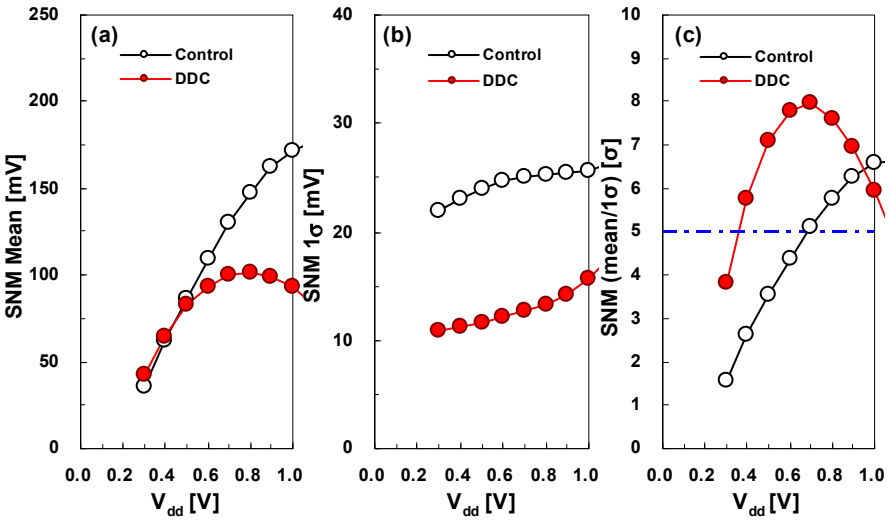

Fig.13 Measured (a) mean, (b) sigma, and (c) mean/1σ of SNM.as a function of V_{dd}.

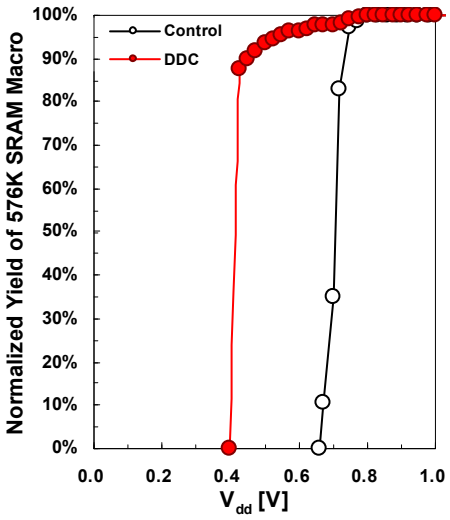

Fig.14 $V_{DD\text{-}min}$ of 576K bit SRAM array. Single bit fail is counted as array fail.