

# C55DDC IP Line-up and Specification

## IP status

ITEM	Features		Provider
Standard cells	ULL Tr. -cell height : 9-track -with body bias control -3 modes (Fast / Medium / Slow)		USJC
	PMC <sup>1)</sup>	Level-Shifter, Isolation, Always-on	USJC
		Power Switch	USJC

PMC <sup>1)</sup>: Power Management Cell

ITEM	Features		Provider
SRAM/ROM	SPSRAM	High Density 1RW (ULL Tr) - with body bias control - 3 modes (Fast / Medium / Retention)	USJC
	ROM	ULL Tr -with body bias Control -3 modes (Fast / Medium / Slow)	USJC

ITEM	Features		Provider
ADC	12bits 1 MS/s		USJC
DAC	10bits 100 kS/s		USJC
ADVbbFS	Body bias control and clock generator 32 KHz–32 MHz		CSEM
PMU	Power supply for 0.6 V / 0.9 V / BLE domain		CSEM
BLE	Version 4.2 and 5 Extended data rate 2 Mb/s, Long Range specification		CSEM

ITEM	Features		Provider
I/O	GPIO use 3.3 V LVt Tr., In-line PAD Type		USJC
	GPIO use 3.3 V HVt Tr., In-line PAD Type		USJC

ITEM	Features		Provider
Plug-In Flash	64 KB-1088 KB ( 64 KB x [0,2,4,8,16] sector + 4 KB x 16 sector )		USJC

## IP specification

All specifications are valid for  $-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$

### ADC

- 12-bit 1 MS/s SAR ADC
- Fully differential input range +/-0.9 V
- Low power consumption

Parameter	Specification	Units
Resolution	12	bits
Conversion rate	1.0	MS/s
Input amplitude (differential value)	+/-0.9	V
Integral linearity error	+/-1.5	LSB
Differential linearity error	+/-1.0	LSB
Total supply power	51.4	$\mu\text{W}$

### DAC

- 10-bit 100 kS/s
- Data generator (sine wave, ramp)
- Low power consumption

Parameter	Specification	Units
Resolution	10	bits
Conversion rate	100	kS/s
Output range	min. $0.167 \cdot V_{DDA}^{1)}$ max. $0.833 \cdot V_{DDA}^{1)}$	V
Resistive output load	min.100	k $\Omega$
Capacitive output load	max.100	pF
Current consumption@no output load	8.5	$\mu\text{A}$

$V_{DDA}^{1)} = 0.9 \text{ V typ}$

### BLE transceiver

A 2.4G-Hz RF PHY IP targeting ultra-low power radio applications

- Bluetooth Low-Energy PHY layer of version 4.2 and 5 including extended data rate 2 Mb/s and long-range specification
- Flexible PHY with data rate up to 4 Mb/s and programmable baseband settings for supporting proprietary modes
- Low-voltage: 0.9 V operation. Supply within 0.85 V-0.99 V range
- No external matching network component
- Very small footprint and very few external components (only XTAL and decoupling capacitor).

Parameter	Specification	Units
Receive mode		
Sensitivity@1Mbps	-97	dBm
Power consumption @0.9 V typ.	5.0	mW

Parameter	Specification	Units
Transmit mode		
TX output power @0.9 V typ.	-0.3	dBm
Power consumption @0.9 V / -0.3 dBm	7.7	mW

### ADVbbFS

Body bias control and clock generator

- 32-kHz Crystal Oscillator
- Digital frequency control loop
- Include the logic/SRAM body bias control method as ADVbbFS
- RTC, Timer, Alarm
- Ring-based clocking source for digital systems

Parameter	Specification	Units
Output clock frequency	0.032 to 32	MHz
Absolute frequency tolerance	-200(min),+50(max)	ppm

### PMU

High-efficiency and ultra low-power management unit

- Regulators for 0.6V / 0.9V / BLE domain
- Inductive buck DCDC converter
- Capacitor-less LDO regulators for RF, analog and digital blocks
- Low-noise bandgap reference
- Ultra-low power current and voltage reference
- Power-on-reset and brown-out detection circuits

Parameter	Specification			
	Min	Typ	Max	Units
Input supply voltage	1.62	1.8/3.3	3.63	V
Output voltage for 0.6 V domain	0.54	0.6	0.66	V
Output voltage for 0.9 V domain	0.81	0.9	0.99	V
Output voltage for BLE domain	0.85	0.9	0.99	V

In collaboration with



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