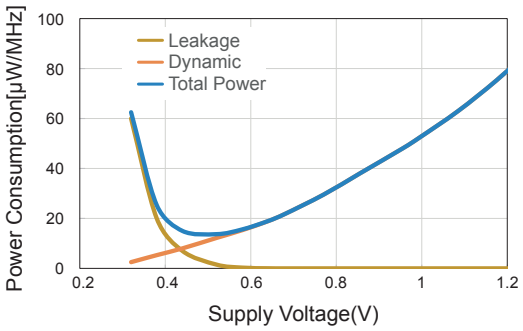
C55DDC Platform for IoT/Wearable Applications

United Semiconductor Japan (USJC) has joined forces with Centre Suisse d'Electronique et de Microtechnique (CSEM) to develop an ultra-low power IP platform targeting near/sub-threshold supply voltages in the USJC's DDC (Deeply Depleted Channel) technology.

Reducing Power Consumption on CMOS

IoT/Wearable devices are normally operated with batteries. In these devices, minimizing power consumption to extend battery life is critical. As the figure below shows, Minimum Energy Point (MEP) is in the sub-threshold region. USJC has been working with CSEM to offer a platform targeting 0.5 V-0.6 V operation.

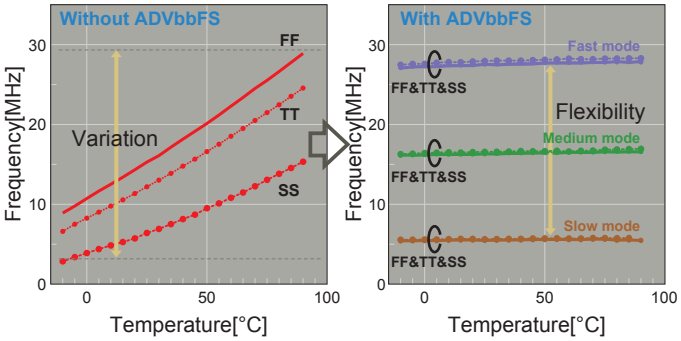


The challenge of near/sub-threshold circuit design

It is well known that circuit performance in near/sub-threshold operations is highly sensitive to variations in the manufacturing process, circuit operation voltage and temperature (PVT). This sensitivity to variation brings difficulties to the circuit design. In addition, the lower supply voltage affects circuit performance and results in lower operating frequency.
USJC's DDC technology addresses these problems effectively and provides a good solution for near/sub-threshold circuit operation.

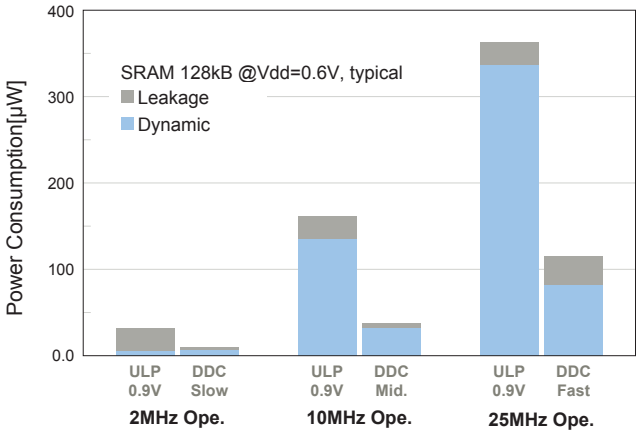
Key features for DDC technology

1) Variation Control and Flexible Performance Tuning



C55DDC utilizes Vbb (body bias) as a means to enable variation control and performance tuning.
The actual Si results for the C55DDC test circuit operated at Vdd = 0.5 V are shown in the lower left figures.
The circuit operation frequency varies widely across process corner and temperature range when Vbb control is turned off.
This frequency variation caused by temperature and process corner can effectively be eliminated when the Vbb control is turned on.
Furthermore, the circuit performance can flexibly be tuned as Fast-, Medium- or Slow-mode by Vbb control regardless of process corner conditions (SS, TT and FF).
This body bias based control scheme is named "Adaptive Dynamic Vbb control and Frequency Scaling (ADVbbFS)".

2) Ultra-Low Voltage Operation : case of SRAM



The body-bias-based control scheme is applied to SRAM Memory and stable operation is realized at near/sub-threshold voltage even with 6T-bit cells. The figure above shows that the power consumption of C55DDC SRAM operated at Vdd = 0.6 V is dramatically lower than that of ULP operated at Vdd = 0.9 V.

C55DDC IP platform for near/sub-threshold circuits

USJC and CSEM release the following IP libraries

- PMU block
  The PMU block consists of DCDC converter and low-power LDO. It takes voltage input from batteries and generates voltages required for each of the power domains.

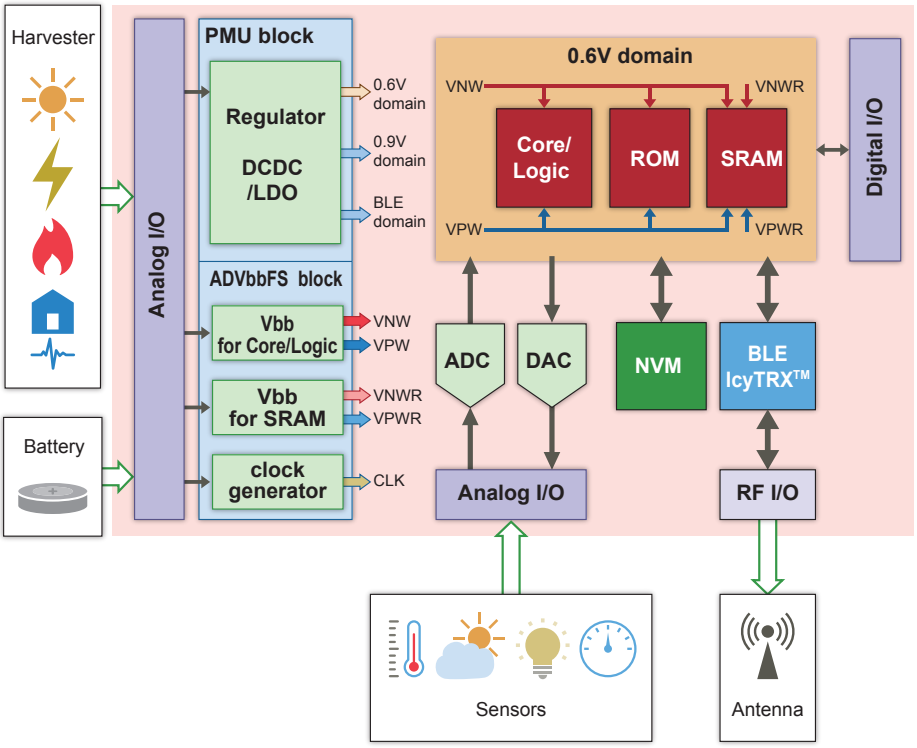
- ADVbbFS block
  The ADVbbFS block supplies Vbb to the core circuits and SRAM memory cell areas. It contains monitors to detect PVT variations and uses the information to compensate the transistor characteristics through dynamically adjusting the Vbb. This reduced variation realizes stable operation even at near/-sub-threshold. Furthermore, the ADVbbFS supports performance tuning through body biasing as well.

- Standard Cells, SRAM and ROM
  These libraries are prepared with built-in body bias based compensation and performance tuning schemes.

- ADC, DAC
  Low-power ADC and DAC macros.

- BLE
  Version 4.2 and 5 including extended data rate 2 Mb/s and long range specification.

- NVM
  64 KB-1088 KB (Plug-in Flash)



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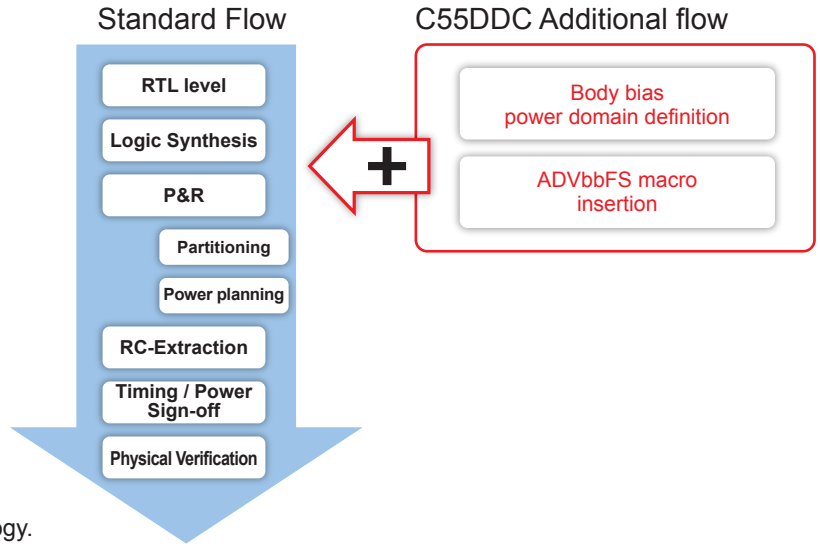
Design flow

- User can design based on the standard flow with two minor additions.

- Additional Flow
  (1) Body bias power domain definition.
  (2) ADVbbFS Macro Insertion

- USJC releases the C55DDC libraries that support Cadence and Synopsys EDA tools.

- USJC releases nine PVT corner libraries.



USJC provides the shuttle service for C55DDC technology.

In collaboration with

csem

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